Test Report for the EDS5108ABTA 3DPLUS ELPIDA SDRAM

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I.   Introduction

This study was undertaken to determine the sensitivity of the 3DPLUS EDS5108ABTA ELPIDA SDRAM to single-event effects using two-photon absorption laser testing and heavy-ion irradiation. The ultimate goal was to determine the suitability of the part and various proposed mitigation techniques for use as a data recorder for health and monitoring data in the Control and Data Handling unit for the Magnetospheric Multi-Scale Mission. The effort was a collaboration between NASA GSFC and Radiation Assured Devices (RAD). Laser testing took place at the Naval Research Laboratory in Washington, DC, and heavy-ion testing was done at the Texas A&M University Cyclotron Facility.

II.   Devices Tested

Two samples of the Device Under Test (DUT) were irradiated and 3 spares were held in reserve for comparison with the irradiated parts if they exhibited anomalous behavior. The DUTs were irradiated with either the laser or the ion beam and observed for errors and destructive conditions. The test samples had datecode 0805.

The 3D+ stacked part is based on an Elpida 512M SDRAM organized as 16,777,216 words x 8 bits x 4 banks. It uses a 3.3V power supply, clock frequency up to 133MHz and can be run with either an auto- or self-refresh. Four banks can operate simultaneously and independently.

III.   Test Facility

Facility: Naval Research Laboratory
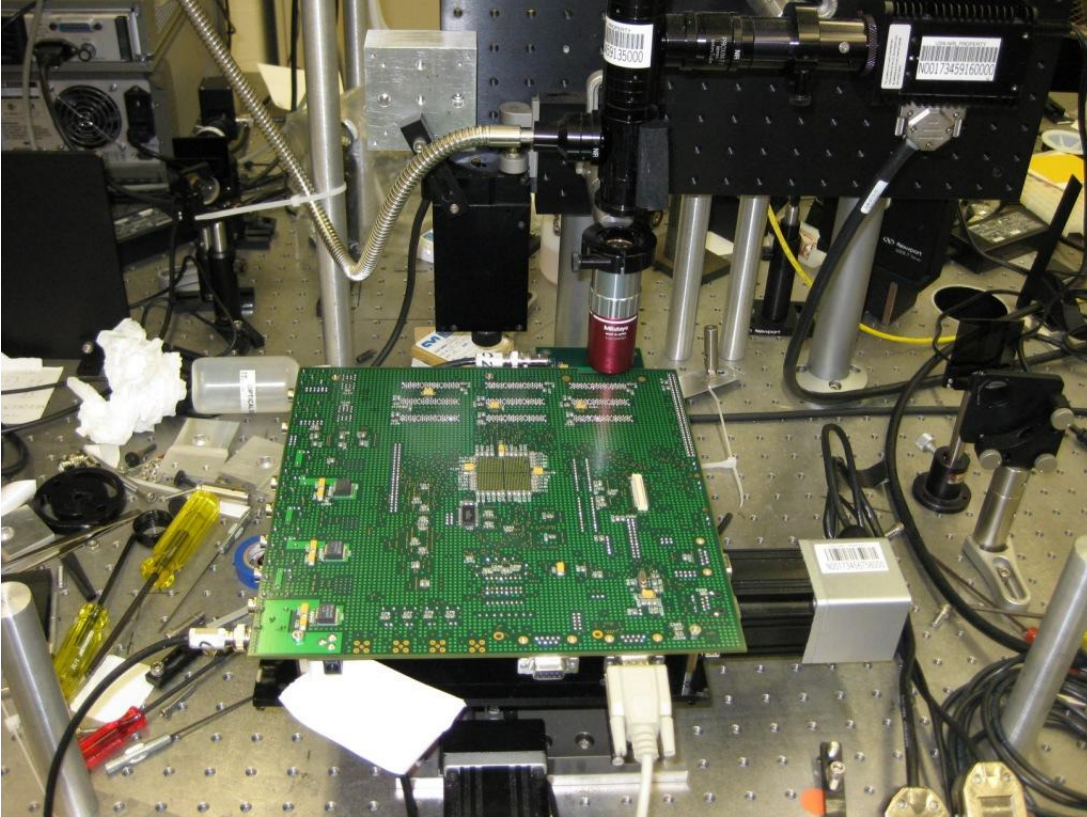**Laser:** 1180 nm (Two-Photon-Absorption—TPA)

Figure 1 TPA laser test facility at NRL, showing the LCDT test board and SDRAM daughter card (upper right of test board) with the objective lens over the DUT.

Heavy-ion: Texas A&M University Cyclotron Facility (TAMU), 25 MeV tune

Table I: Test ions at TAMU

Ion-Energy (MeV)	Incident LET (MeVcm^2/mg)	Range in Si (µm)
Ne-545	1.7	799
Ar-991	5.4	493
Kr-2081	19.3	311
Xe-3197	37.9	286

IV. Test Conditions and Error Modes

Test Temperature: Room Temperature and 85 degrees Centigrade (maximum operating temperature)

Test Patterns:
    00   [00000000]
     FF   [FFFFFFF]
     55   [01010101]
     AA   [10101010]
     AA55   [10101010] [01010101]

PARAMETERS OF INTEREST: Control logic and memory cells Values, and power supply currents

Error Conditions: SEU, Block/Logic errors, SEFI (previous testing revealed this part is not SEL susceptible)

V. Test Methods

Device Control: In all tests, the SDRAMs were mounted on daughter boards that were interfaced to the FPGA-based Low-Cost Digital Tester. (See figure 2.) The tester provided all clock and control functions for the DUT during testing. GPIB control was provided by a laptop.

Laser Testing: The devices were tested in the five test patterns listed in section IV. A pattern was selected, written to the memory and verified. The laser beam was then focused on the active volume of the part and scanned over it for sensitive regions. When a sensitive area was found, the number and character of errors caused was investigated, along with the threshold laser intensity for onset of errors. In addition to manual scanning, we also had the option to raster over a sensitive area to zero in on the most sensitive features.

The LCDT read data from the memory, and if the data deviated from the expected pattern, the address, error value and expected value were recorded and the error counter was incremented. The error would be overwritten with the correct data pattern if possible. In the event that a burst of errors was seen, the beam would be blocked and the output of errors would be monitored to see if all the errors were correctable and functionality restored. In the event that the error could not be overwritten or that functionality could not be restored, the event was designated a SEFI and we would try to recover functionality—first by rewriting the mode registers, then by a DUT reset and finally by cycling power to the device.

Testing would be done according to the following test procedures:

Read-Modify-Write:
Send Reset
Select Data Pattern
Set Data Pattern
Send Command
Write pattern
Start, Read continuously
  If error, correct or rewrite and record data

Read-Only:
Send Reset
Select Data Pattern
Set Data Pattern
Send Command
Read Only switch up
Write Pattern
Start, Read continuously
  If error, do not correct
  Error is read over and over again
  Not trying to fix error

Read-Read-Modify-Write: (Double-Read):
Send Reset
Select Data Pattern
Set Data Pattern
Send Command
Double Read switch up
Write Pattern
Start, Read continuously
        If error, read again, if second error correct or rewrite and record data
        If error, read again, if no second error do nothing

Refresh Mode Register:
        Misc Command
        Send Command
        Refresh Long to refresh

In previous testing (by Radiation Assured Devices), the following types of errors were found:

Type 1: An error is detected with no loss of functionality of the device. The error looks like a "regular" SEU event (bit flip), but is recovered via mode-register reset (with no data loss or need to re-write the bad bit).

Type 2: A functional error is detected (continuous bad data) that is recoverable with a mode register reset. After the mode register reset there is no data loss.

Type 3: A functional error is detected (continuous bad data), the errors are not recoverable with a mode register reload and the data needs to be re-written. This type of SEFI could be caused by an internal decode register or possibly a corruption of the auto-refresh register/counters leading to data loss or corruption.

Type 4: An error is detected and the errors are not recoverable with a mode register reload (data loss occurs, same as SEFI Type 3). In addition, the data cannot be immediately re-written and a "re-start" or "wait-state" is required to regain control. Note that at this time a "re-start" is defined as the need to issue a series of "no-op" commands prior to reloading the mode register to the device and retesting for functionality until the device functions properly (note that the "no-ops" last for approximately 10µs).

Heavy-Ion Testing: Heavy-Ion testing used the same patterns and test procedures as those used for laser testing. However, because of the high susceptibility to block errors revealed by laser testing, we opted to test using very short, low-fluence runs (<100 ions/cm^2). The low-fluence runs decreased the likelihood that multiple SEFIs occurred in the same run and produced enough runs without a SEFI (especially at low LET) to calculate a realistic SEU rate. In addition, testing was done for angles of incidence at 0° and 45° to the normal. In the case of heavy-ion testing, the vast majority of runs ended with a block error or other large error. As such, at the end of the run, we carried out the same recovery procedures listed under the description of laser testing.
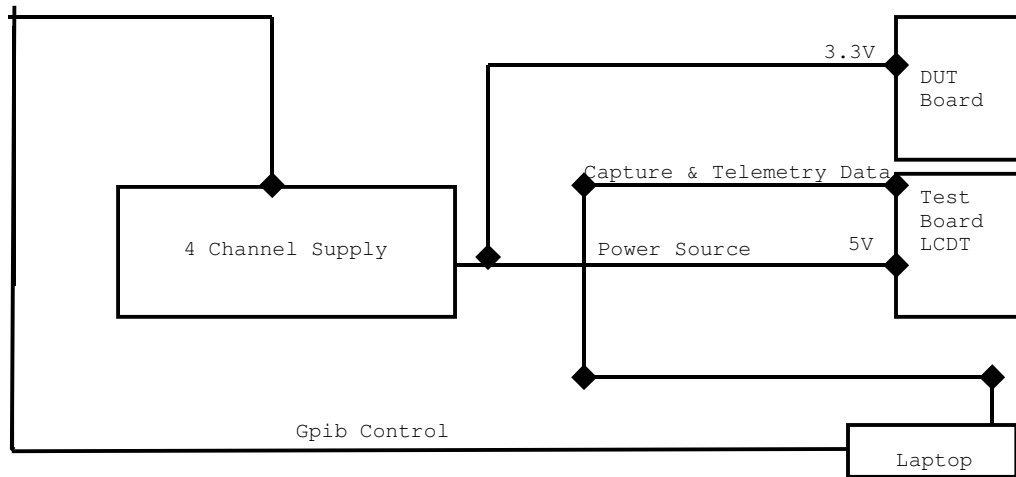
Figure 2. 3DPLUS ELPIDA SDRAM ESD108ABTA Overall Block Diagram for laser testing

VI. Data Analysis

Data analysis for SDRAMs is labor intensive. Although the types of errors are common from one SDRAM to the next, the signatures may vary, and the large memory size means that there is often a significant delay between when an error occurs and when it is discovered. This means that separating the different error modes requires sorting through the data by hand. Errors were grouped into SEU (single isolated errors), logic errors (<100 words corrupted in a burst), block errors (>100 words corrupted in a burst and sharing a common Row or Column) and burst errors (errors occurring at the same time, but at seemingly unrelated addresses). In addition, if errors did not recover automatically, they were designated SEFI, or, if accompanied by an increase in current, SEL.

VII. Results and Discussion

Laser testing: Laser testing revealed several facts that would have been difficult to determine by heavy-ion or proton testing alone. First, the critical charge for upset of control logic was up to 2x lower than the critical charge for upset of memory cells. Laser testing also revealed precisely one SEFI. Despite a systematic automated search of the region where the SEFI occurred, the event was not repeatable. Moreover, detailed analysis of the errors captured for the event showed that the error signature was indistinguishable from a long series of column errors. This suggests that the SEFI vulnerability occurs only during a limited operational or temporal window, and that these errors should be rare. We also note that none of these errors were seen during low-frequency operation (10 MHz) that will be characteristic of the MMS application. Other than this event, all SEE modes were recoverable. Most locations in the memory array

yielded SEUs, although we also found control logic in the memory array that yielded logic errors resulting in corruption of a few data words per error (see figure 3).
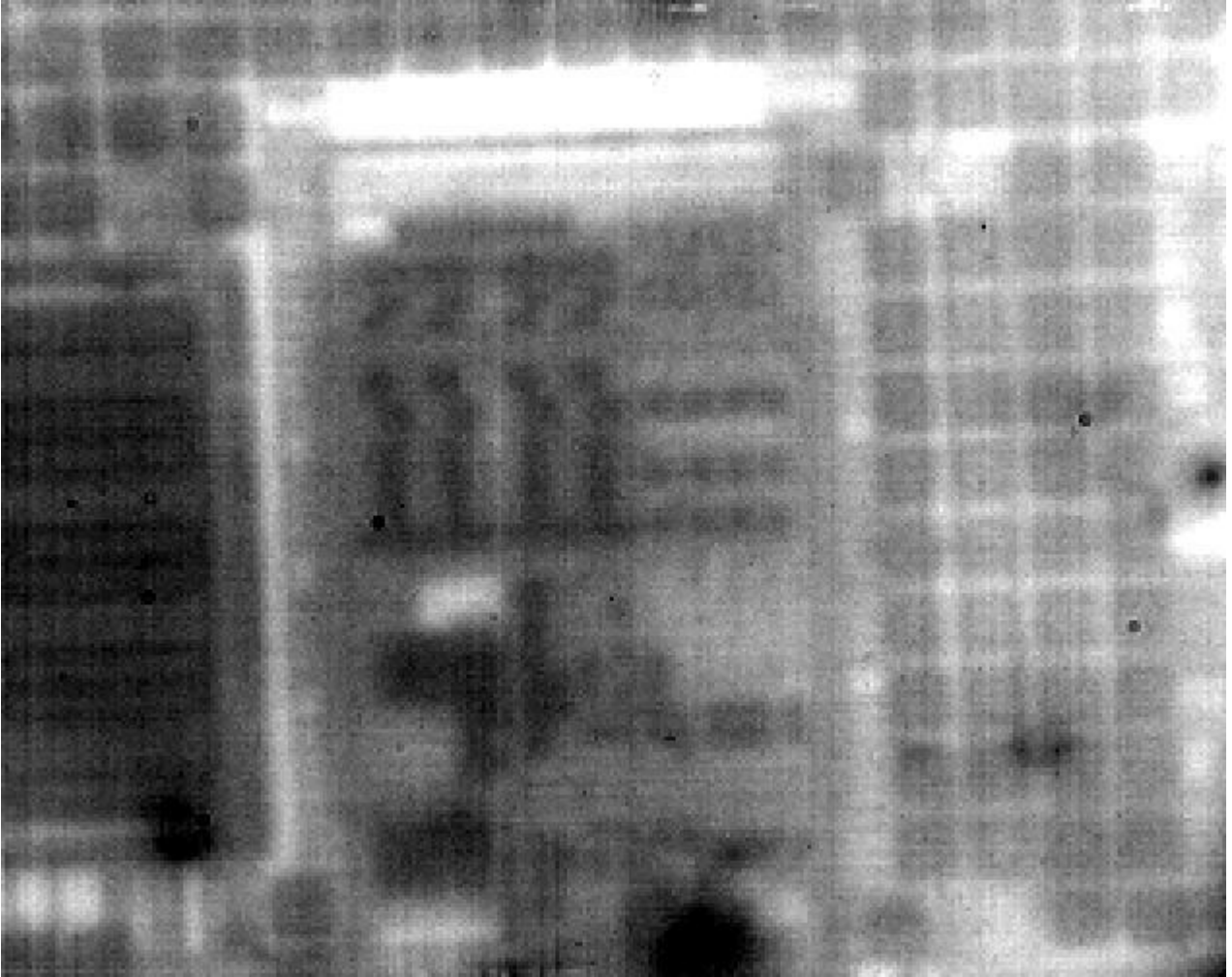

Figure 3 Control logic in the memory (central portion of IR photo) produced logic errors with 1-20 words corrupted per error. Squares on either side of the control logic are the memory elements. Individual memory cells are too small to resolve at this scale.

In some cases, control logic gave rise to events that were indistinguishable from SEUs, except that repeated reads showed that the affected address was not really in error. These errors likely contaminate most SEU cross section estimates, but the area of the control logic is small compared to the memory area.

However, most of the control logic was located in a strip running down the central portion of the chip. The most sensitive portions of control logic appeared in the IR micrograph as comb-like structures (see figure 4).
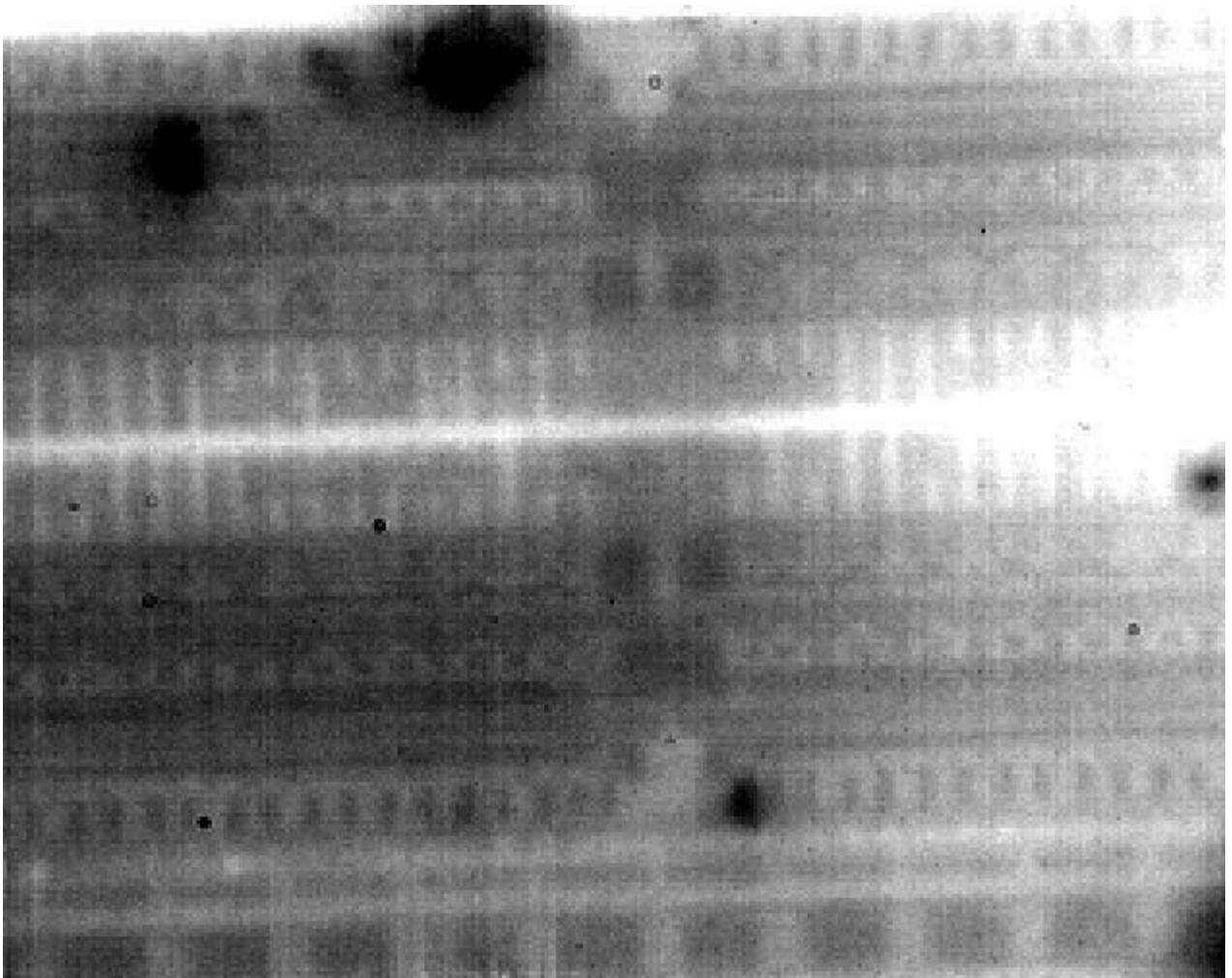
Figure 4 Comb-like structures in the control logic running along a central strip produced logic errors and block errors (both column and row). The control logic had an upset threshold critical charge just over half that of memory cells.

A representative survey of several SEE susceptible locations in the control logic (see figure 5) found that the majority of error modes produced only a few dozen words in error, but that error bursts as large as 4096 were possible. All such errors were correctable. The average control logic upset produced about 200 upsets.
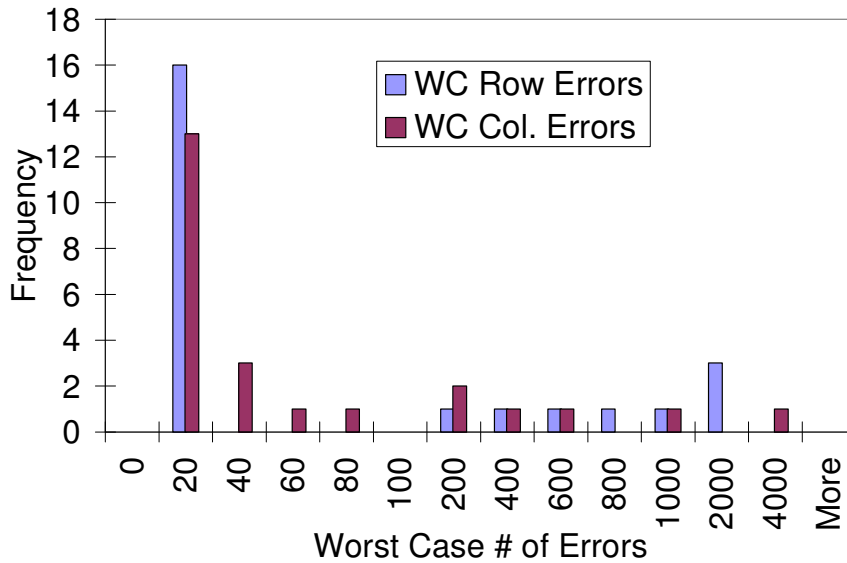
Figure 5 Distribution of the frequency of worst-case number of errors for representative locations in the control logic of the Elpida 512 Mbit SDRAM.

The upset numbers are useful in determining refresh rates for the application.

Heavy-Ion Testing: Although TPA laser testing was invaluable for enumerating the types of effects to expect from errors in the SDRAM, estimating the rates at which these effects occur requires heavy-ion data. We also verified that the heavy-ion error types were consistent with those seen during laser testing. Figure 6 shows the cross section vs. LET curves for SEU, small logic errors (<20 errors) and block errors (>20 errors)
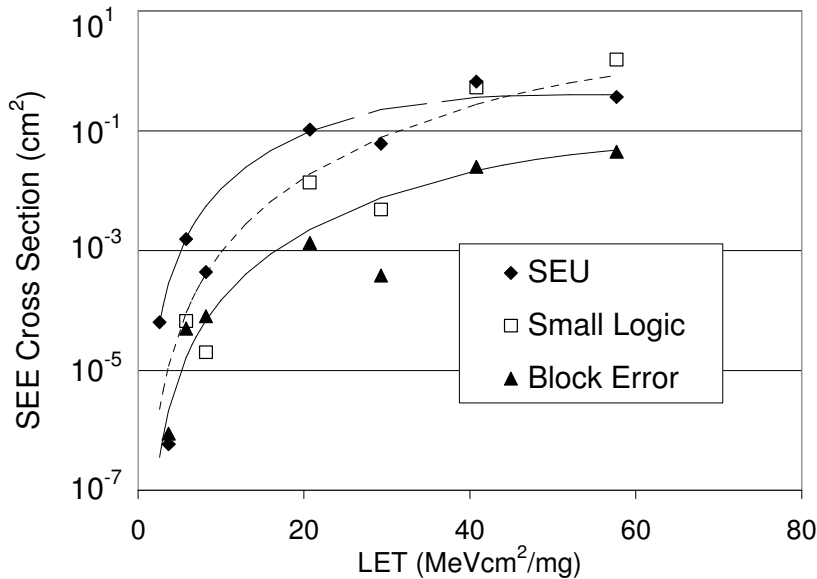

Figure 6 Cross section vs. LET for SEU, small logic and block errors. Curves represent fits to the data.

From figure 6 it is clear that the susceptibilities to SEU and small logic errors will be nearly equal. It should also be noted that the device will likely exhibit all three types of errorsl due to protons.

One SEFI was also observed during heavy-ion testing, although it manifested somewhat differently from that seen in laser testing. This event was also consistent with the susceptibility being time dependent. Although the event occurred at an LET of ~20 Mevcm^2/mg, it is not possible to guess the saturated cross section or onset from this information. It is likely that the rate for such events will be much less than the rate for block errors.

VIII.   Conclusion

Based on the results above, it is likely that the SDRAM will be adequate for the MMS mission given the Reed-Solomon error correction code and interleaving used in the application. Block errors, logic errors and SEU should not contribute significantly to errors in this application. Of somewhat more concern are the functional interrupts seen in both laser and heavy-ion testing. These parts would require a power cycle to clear, resulting in the loss of contents of the memory. Depending on how the application is implemented, this could mean loss of half the data for the affected period. One possible mitigation for this error would be to alternate the bank in which telemetry readings are stored. This would result in loss of only every other reading.

Estimating the rate at which these SEFI would occur is difficult, because we only observed one such event during both laser testing and heavy-ion testing. A best estimate based on these admittedly slim statistics would suggest that the constellation of satellites could see one or two such events during the mission. However, we note that these events were only seen when the part was clocked at high speed, and the inability to reproduce these events despite knowing the general susceptible region for the laser test suggests that the error susceptibility is time or state dependent. This means that the rate could be quite low for the lower application speeds of the MMS application. Project engineers have indicated that such performance is acceptable in the application and have no plans for additional mitigation.